D/A LADDER CALIBRATION USING A LINEAR VOLTAGE TO FREQUENCY CONVERTER BASED ON THE DUAL INPUT PHASE ACCUMULATOR

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ABSTRACT:

This paper presents a new Voltage to Frequency Converter (VFC) and its use for the calibration of high-resolution high-accuracy converters. The VFC is a PLL based frequency synthesizer that employs a Dual Input Phase Accumulator (DIPA) that behaves as a linear phase detector.

The DIPA has two digital inputs, one for the reference (Fref) frequency and one for the VCO frequency (Fout). Additionally, the DIPA has two voltage (analog) inputs, so called Vref and Vin. The DIPA's output is linearly proportional to the integral of the difference (Fref.Vin - Fout.Vref). Therefore output frequency of the DIPA based synthesizer is controlled linearly from the Vin input, since the DIPA based PLL keeps the ratio of the two frequencies Fout/Fref equal to the ratio of the two input voltages Vin/Vref. The accuracy of synthesized frequency of the DIPA based VFC does not depend on accuracy of the capacitors and the other components employed for its implementation, but on its ratio, in contrast to the conventional VFC. Additio-nally, the convergence speed, the phase noise and the performance of the DIPA based analog synthesizer is enhanced compared to these of the conventional PLL based synthesizer.

The DIPA based VFC can be used for the calibration of a high-resolution D/A ladder. The frequency ratio can be digitally measured at high accuracy and subsequently the voltage ratio is estimated at the same accuracy.

1. INTRODUCTION

In this paper, an enhanced PLL based Voltage to Frequency Converter (VFC) it is pre-

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sented. The core of the VFC is an analog, Dual Input Phase Accumulator (DIPA) that behaves as a linear phase detector. Additionally, a VCO and an LPF are employed to form the VFC. The output frequency of the VFC is linearly proportional to the input reference frequency and to the ratio of the input voltage and a reference voltage.

DIPA has two frequency inputs and two voltage inputs. The frequency (digital) inputs to the DIPA are a constant frequency (Fref) and the VCO output frequency (Fout). The voltage inputs to the DIPA are the input voltage (Vin) and a reference voltage (Vref). The output of the DIPA is linearly proportional to the integral of the normalized frequency difference $F_{ref} \cdot V_{out} - F_{out} \cdot V_{ref}$; thus, it is proportional to the normalized phase difference of the two input frequencies.

The DIPA samples and calculates the phase difference of the two input frequencies at very high rates. This results to an analog frequency synthesizer with enhanced characteristics on the convergence speed, phase noise, spurs and resolution. The two input clocks of the DIPA correspond to the reference and the output frequency and applied without normalization (division) to the Fstep frequency, as the conventional phase detector requires.

DIPA is an enhanced, low-power, low-cost, high-frequency phase detector, and can be used for frequency synthesis and for high accuracy Voltage to Frequency and Frequency to Voltage converters.

In this paper, the use of the DIPA based Voltage to Frequency Converter (VFC) for the calibration of a high resolution D/A ladder is demonstrated. The ratio of the two frequencies (Fout/Fref) can easily be measured digitally at the required high accuracy using conventional technology (counters). Therefore, the ratio Vin/Vref is also estimated at the desired accuracy.

2. THE PRINCIPLE OF THE ANALOG DIPA

The principle of the analog implementation of the DIPA is depicted in Fig. 1. The capacitor C1 is charged through the switch S1 when the Fref input is High. When the Fref input is Low, the C1 is discharged on the input of the integrator through the switch S2.

Considering that Vref is a positive voltage and Vin is a negative one, the mean current from the integrator's input due the input frequency Fref is:

$$Iref = Fref \times Vin \times C1 \tag{1}$$

Subsequently, the mean current to the integrator's input due the output frequency Fout is:

$$Iout = Fout \times Vref \times C2 \tag{2}$$

Therefore the output of the integrator (V_{DIPA}) is proportional to the normalized phase difference of the two input frequencies and is given by the equation:

$$\begin{gathered} V_{DIPA} = \frac{1}{C3}\int \left(Fout \times Vref \times C2 - Fref \times |Vin| \times C1 \right) dt = \\ V_{DIPA} = \frac{C2 \cdot Vref}{2\pi \cdot C3} \cdot \left(\varphi out - \varphi ref \times \frac{|Vin|}{Vref} \times \frac{C1}{C2} \right) \end{gathered} \tag{3}$$

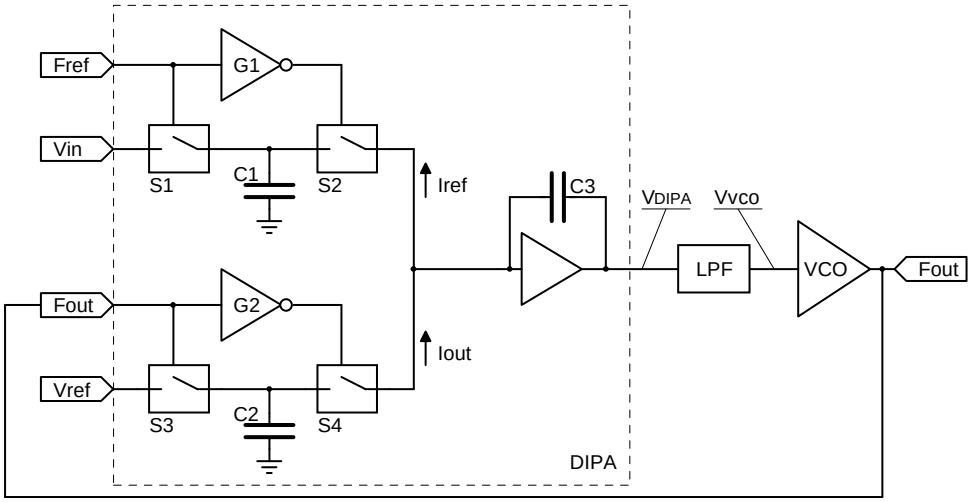

Fig. 1. The principle the analog DIPA based VFC

When the synthesizer is locked, the mean current at the input of the DIPA's integrator is zero, and the following equation is true:

$$Fref \times |Vin| \times C1 = Fout \times Vref \times C2 \tag{4}$$

Therefore, the output frequency of the synthesizer can be controlled linearly, by controlling the voltage Vin. Additionally, the ratio Cr=C1/C2 is a constant value and thus the expression for the output frequency can be simplified as:

$$Fout = Fref \times \frac{|Vin|}{Vref} \times Cr \tag{5}$$

The DIPA output consists of a DC component proportional to the normalized phase difference of the two input frequencies and high frequency harmonics of the two input frequencies, [3]. The transfer function of the DIPA is linear and monotonic [3] and its gain is:

$$Kd = \frac{Vref \times C2}{2\pi \times C3} Volts / Rad \tag{6}$$

DIPA can be considered as the only phase detector that can handle phase differences more than 2π. Additionally, DIPA can be considered as the only phase detector that can measure the phase difference of two not equal frequencies without prior normalization down to a frequency which is the common denominator of the two input frequencies.

The wide band LPF employed in the DIPA based VFC, reduces the high frequency harmonics mentioned above and on the same time does not reduce the high convergence speed of the loop. The behavior of the DIPA based VFC is identical to the conventional PLL based synthesizer, therefore the parameters of the LPF can be easily calculated using the conventional PLL theory, [1], [2], [4].

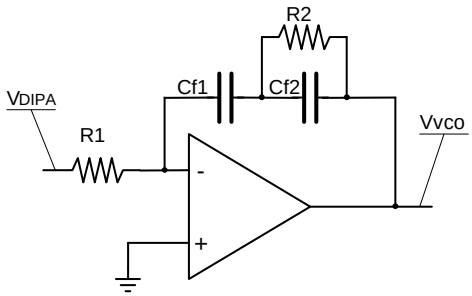

Fig. 2. The preferred filter for the DIPA based VFC

3. CONSIDERATIONS ON THE ACCURACY OF THE VFC.

Several factors affect the accuracy of the synthesized frequency. In this section, the most important of them are considered.

3.1. THE QUALITY OF THE INTEGRATOR

The current loss on the capacitor C3 employed in the integrator of the DIPA may introduce significant frequency error. The use of the active filter depicted in Fig. 2, as the filter of the PLL eliminates the DC voltage on the capacitor C3, eliminating at the same time the need for a high quality capacitor.

The finite gain of the op-amp does not affect the proper operation of the integrator. However, a high slew-rate, wide unity-gain-bandwidth op-amp is required to ensure the quality of the virtual ground at the input of the integrator. Experimentally has been confirmed that the accuracy of the VFC is significantly improved, as the gain Kd of the DIPA is reduced (increasing the capacitor C3).

3.2. THE VOS OF THE DIPA'S INTEGRATOR

The offset voltage of the op-amp employed in the integrator of the DIPA affects seriously the accuracy and the linearity of the VFC. Due to the Vos, the capacitors C1 and C2 are not discharged to the ground as required but to the Vos. Therefore the output frequency due to the Vos is:

$$Fout_{Vos} = Cr \times Fref \times \frac{|Vin| + Vos}{Vref - Vos} \tag{7}$$

The Vos introduces a frequency error that is given by the equation:

$$Ferr_{Vos} = 10^6 \cdot \frac{Vos \cdot (Vref + |Vin|)}{Vref \cdot (Vref - Vos)} \; PPM \tag{8}$$

The frequency error that is given in Parts Per Million (PPM) will be as low as the input voltage Vref bigger than the Vos. However, Vos always introduces a frequency error which can be as much as some thousands PPM. Therefore, Vos cancellation techniques should be used to eliminate the Vos and subsequently the introduced frequency error.

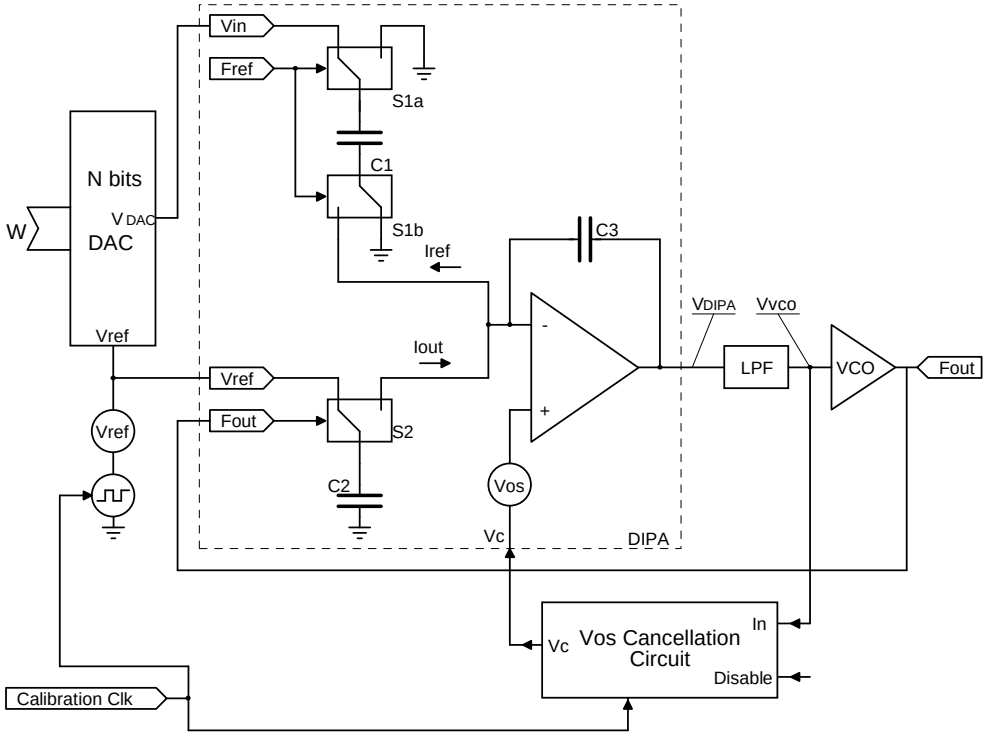

Fig. 3. The indirect Vos cancellation technique for the DIPA based VFC

An indirect Vos cancellation technique for the DIPA based VFC has been developed and demonstrated in this paragraph. In Fig. 3 the DIPA has been modified so as to operate with positive voltages to both analog inputs. For the generation of the Vin, a DAC has been employed to be able to adjust at a constant value the Vin/Vref ratio.

On the Vref voltage source applied to the DIPA and the DAC, a square-wave voltage source is added. Therefore, Vref has two voltage levels the Vref(0) and the Vref(1). Consequently, the Vin input to the DIPA will have also two voltage levels Vin(0) and Vin(1). The ratio Vin()/Vref() is constant and is depended on the digital input word (W) to the D/A ladder, on the number of the bits (N) of the ladder ($K=W/2^N$) and on its accuracy. The Vvco output of the filter that drives a VCO with gain Kv, will be a square wave with amplitude:

$$\Delta\mathrm{Vvco} = \frac{1}{\mathrm{Kv}}\left(Fout(0) - Fout(1)\right) = \frac{Cr \cdot Fref}{Kv} \cdot \frac{Vos \cdot (1+K) \cdot \left(Vref\,(1) - Vref\,(0)\right)}{\left(Vref\,(1) - Vos\right) \cdot \left(Vref\,(0) - Vos\right)} \qquad (9)$$

According to the above equation, the Vos cancellation circuit should adjust the Vos cancellation voltage Vc so as to zero the ΔVvco. Additionally, it can be found from the same equation that the ΔVvco is a square wave of the same phase to the input source, if the Vos is positive, whereas it is inverted if the Vos is a negative voltage.

The calibration clock that controls the calibration circuit and the square wave voltage source should be slow enough, having a period bigger than the convergence time of the loop.

The Vos cancellation circuit is a simple high-gain circuit that feedbacks at the positive input of the op-amp employed in the DIPA's integrator, an equal and negative to Vos voltage.

In this point, it should be emphasized that during the convergence of the VFC to a frequency the Vos cancellation circuit should not function keeping the Vc voltage at the previously estimated level. Therefore, the Disable input to the Vos cancellation circuit should be active during the convergence of the VFC.

3.3.THE IMPERFECTION OF THE SWITCHES

The imperfections of the MOSFET switches used to charge and discharge the capacitors C1 and C2 affect the accuracy of the synthesized frequency. The most important factors are the Ron and Roff resistance of the switches and the charge inserted to the capacitors C1 and C2 due to the parasitic capacitances of the gate of the MOSFETs.

The Ron resistance of the switches does not allow the capacitors C1 and C2 to be fully charged and discharged. Assuming that Ft is the frequency derived by the Ron resistance of the switches and the capacitors C1 and C2 ($Ft=1/(2\cdot\pi\cdot Ron\cdot C1)$), the frequency error introduced is given:

$$Ferr_{Ft} = 10^6 \cdot \left(\frac{1 - e^{\frac{\pi Ft}{Fref}}}{1 - e^{\frac{\pi Ft}{Fout}}} \right)^2 \; PPM \tag{10}$$

However, it is has been proven, [3], that this frequency error is negligible when the input frequencies are about ten (10) times less than the Ft. Equally negligible is the error introduced due the Roff resistance of the switches. The frequency error introduced by the Ron and Roff resistance of the switches is not more than 50 PPB (Parts Per Billion).

The charge inserted in the C1 and C2 through the parasitic capacitances of the MOSFET affects the accuracy of the VFC identically to the Vos, therefore the Vos cancellation circuit will reduce the effects of this phenomenon. However, several techniques can be used to reduce further this phenomenon. The capacitors C1 and C2 should be significantly larger than the parasitic capacitances of the MOSFET. Additionally, the use of a dummy MOSFET in series to the switch that has complementary input at its gate and the reduction of the slew rate of the control signal, are techniques already being in use, reducing successfully the effects of this phenomenon.

4. D/A LADDER CALIBRATION SCENARIO

In this section, the use of the DIPA based VFC for the calibration of a high resolution D/A Ladder is demonstrated. To calibrate an N-bits D/A Ladder is required to measure the contribution of each bit to the output voltage. Therefore, it is not required to measure the voltage ratio for all the 2^N possible digital inputs. Only N measurements are required to de-

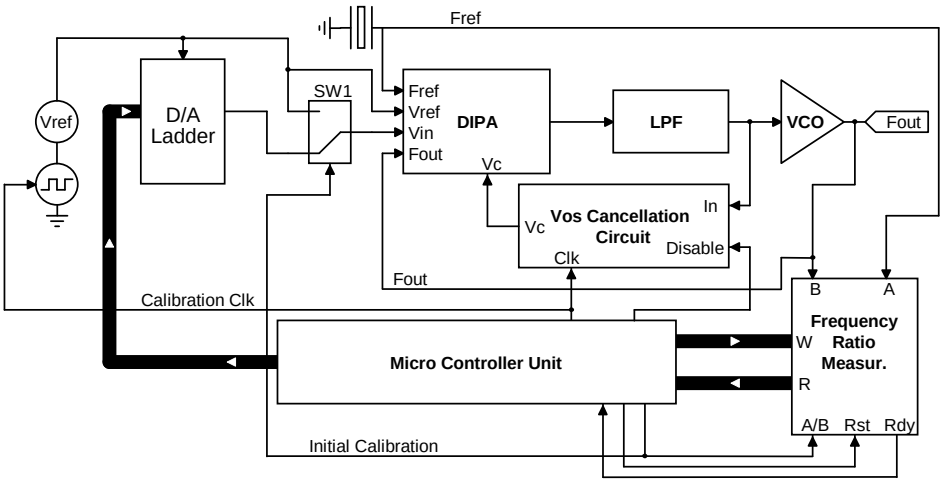

Fig. 4. The D/A Ladder calibration circuit

termine the contribution of each bit to the output voltage. The block diagram of the circuitry required for the calibration is depicted in Fig.4.

In order to keep the VCO output frequency in a reasonable range the most significant bit of the digital input of the ladder should be always on. The frequency range of the VCO employed in the VFC should include the range (Fref/2 - Fref).

The micro-controller unit (MCU) should measure the frequency ratio for N different outputs of the D/A ladder and store them in its RAM for further processing. The list of the N different digital inputs applied to the digital input of the ladder is:

$$(2^{N-1}, 2^{N-1}+2^0, 2^{N-1}+2^1, 2^{N-1}+2^2, \ldots\ldots\ldots 2^{N-1}+2^{N-3}, 2^{N-1}+2^{N-2})$$

For each frequency ratio measurement the MCU should apply to the digital input the proper digital word and should wait for enough time so as the output voltage of the ladder and the output frequency of the VFC is settled. Afterwards, resets the Frequency Ratio Measurement system (FRM) and waits until the frequency ratio is measured (Rdy signal). Finally, MCU stores this ratio in its RAM. When all the required measurements are acquired, the MCU is able to calculate the parameters and the performance of the D/A ladder.

The simplified schematic of the FRM circuit depicted in Fig. 5 employs two counters and counts in the counter B the number of the pulses of the input frequency B occurred in a constant time interval. This, is assigned as the time interval required for the counter A to count a constant number of pulses (W) of the input frequency A . The output of the FRM circuit is a digital word (R) that is proportional the ratio of the two input frequencies.

The FRM circuit is useful for the initial calibration required for the DIPA based VFC. The Cr ratio of the two capacitors employed in the DIPA is too costly to be manufactured at the required value within the required accuracy. It is preferable to measure it initially, at the required accuracy and consider it for the accurate operation of the DIPA based VFC. Therefore, the Cr ratio should be measured initially, applying at the W input of the FRM the digital full-scale value (2^N) of the D/A ladder. On the same time, we have to activate the 'Initial Calibration' signal so as to apply the same input voltage (Vref) to both analog inputs

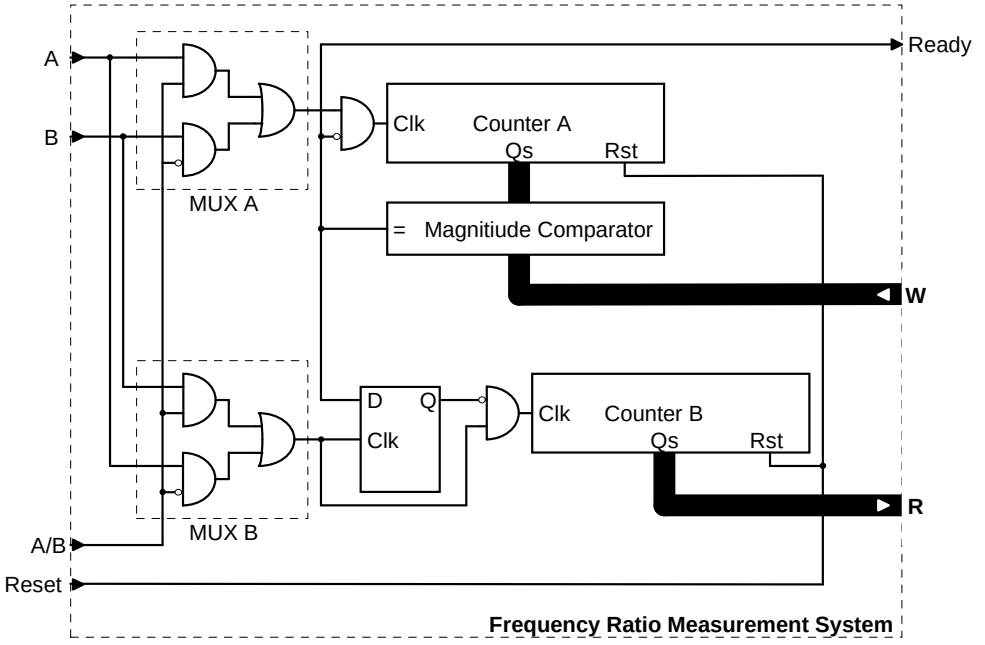

Fig. 5. The Frequency Ratio Measurement circuit

of the DIPA by controlling the switch S1 depicted in Fig. 4. Additionally, the Initial Calibration' signal exchange the frequency inputs to the FRM internally using the multiplexers MUX A and MUX B, depicted in Fig. 5. Therefore, activating the 'Initial Calibration' signal, the output digital word R_{Cr} of the FRM system is the number of pulses of the Fref frequency counted in the Counter B, in the time interval the Counter A counts 2^N pulses of the frequency Fout. The digital word R_{Cr} is related to the Cr ratio:

$$\frac{R_{Cr}}{2^N} = Cr \tag{11}$$

The measurements required for the calibration of the D/A ladder should take into account the ratio Cr and should use as input to the digital word W of the FRM the digital value R_{Cr}.

The number of bits employed in the FRM system is required to be at least one more the number of bits of the D/A ladder. Increasing the number of bits of the FRM system, the accuracy of the measurement of the frequency ratio is increased, however, the required time for the measurement is also increased.

5. CONCLUSION

In this paper, we presented a very accurate Voltage to Frequency Converter based on a PLL that employs the Dual Input Phase Accumulator. It has been proven that this VFC can keep the ratio of two voltages equal to a ratio of two frequencies at very high accuracy. An

enhanced method for the indirect cancellation of the frequency error occurred due to the use of imperfect analog components (op-amps) has been introduced. Additionally, a method for the calibration of a high-resolution D/A ladder has been proposed.

The core of the VFC is the Dual Input Phase Accumulator that samples and normalizes the phase of the two input frequencies at very high rate. This, results to a phase detector with a wide, linear and monotonic transfer function and low-noise at its output. These DIPA's properties facilitate the design of an enhanced voltage-controlled frequency synthesizer with high (linear) resolution, high-convergence speed and low phase noise.

The DIPA based PLL can be used in a wide area of high accuracy applications based on the voltage ratio, the frequency ratio and/or the capacitance ratio.

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